UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/616,144	07/13/2000	Van Hoa Lee	AUS9-2000-0311-US1	4740

7590 01/30/2004

Duke W Yee
Carstens Yee & Cahoon LLP
P O Box 802334
Dallas, TX 75380

EXAMINER	
BANANKHAH, MAJID A	
ART UNIT	PAPER NUMBER
2127	2

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/616,144	LEE, VAN HOA	
	Examiner	Art Unit	
	Majid A Banankhah	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. This office action is in response to application filed on July 13, 2000, Claims 1-26 are considered for examination.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kauffman (U.S.Pat. No. 6,633,916, hereinafter Kauffman) in view of Mason et al. (U.S.Pat. No. 5,319,760, hereinafter Mason)

Per claim 1, Kauffman teaches:

A data processing system (Fig. 1), comprising: a plurality of hardware devices (col. 4, lines 34-45, The single physical machine with multiple physical processors and resources is adaptively subdivided by software into multiple partitions); a plurality of operating systems (col. 4, lines 34-45, multiple instances of operating systems execute cooperatively in a single multiprocessor computer wherein all processors and resources are electrically connected together); and a firmware component for partitioning the plurality of hardware resources (Fig. 3, memory and I/O devices) for interaction with the plurality of operating systems (Title, virtual resource handling, and Fig. 2, 208, 210, 212).

The reference of Kauffman he fails to explicitly teach of the firmware component is implemented using 64-bits. However, the reference of Mason teach of virtualization firmware for operating on a CPU, where the entries for the pages are remained in the translation buffer when

making a context switch between processes or between virtual machines (Mason, col. 2, lines 47-68, When executing virtual machines on this CPU, with a virtual machine monitor, the address space match feature is employed within a virtual machine, but an additional entry is provided to disable the address space match feature for all address space numbers for the virtual machine monitor. In another embodiment, an additional entry is provided in the translation buffer to restrict the address space match feature to those address spaces associated with a single virtual machine or virtual machine monitor). Additionally, mason teach of using a data paths and registers within the CPU (CPU 10) which are generally **64-bits** or quadword size, and the memory 12 and caches use the quadword as the basic unit of transfer for the reason that performance is enhanced by allowing only quadword or longword loads and stores (See, Mason, col. 6, lines 15-16, **The main data paths are registers in the CPU 10 are all 64-bits wide**, and col. 8, lines 47-49, Referring to FIG. 8, **the format 76 of the virtual address asserted on the internal address bus 56 is shown. This address is nominally 64-bits in width**). Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use **64-bit firmware of Mason** (64 Register bits or quadword size) in the **Virtual Resource Handling system of Kauffman** because, it enhances the performance of the virtualization component.

Regarding the zero extension of 32-bit value into 64-bit values in claims 9, 15 and 21, See Mason in col. 6, lines 31-35, and col. 8, lines 5-9.

Per claims 2, Kauffman teaches of the plurality of hardware devices comprise a plurality of processors in Fig. 1 (102, 106), and he teaches of processors operating in a 64-bit mode (See Kaufman, col. 10, lines 34-41).

Per claims 3, 13-14, 19-20, and 25-26, the firmware component comprises a firmware kernel and the firmware kernel maintains a list of address and size pairs that describe cacheable system memory addresses (See Mason, col. 4, lines 41-58, If the page table entry (PTE) associated with the virtual address from the virtual PC is cached in the TB 36 then the page frame number (PFN) and protection bits for the page which contains the virtual PC are used by the instruction unit 18 to complete the address translation and access checks. A physical address is thus applied to the address input 37 of the instruction cache 21, **or if there is a cache miss** then this instruction stream physical address is applied by the bus 38 through the address unit 19 **to the cache 20 or memory 12**).

Per claims 4-5, the data processing system as recited in claim 4, wherein the primitive method, responsive to a determination that the address is cacheable, carries out the method using an appropriate machine language instruction (Mason, col. 4, lines 48-58, if there is a cache miss then this instruction stream physical address is applied by the bus 38 through the address unit 19 to the cache 20 or memory 12).

Per claim 6, the reference of Mason teaches of enabling a real mode cache-inhibit mechanism on one of the processors and allows the access to the address to be performed by machine language instructions within one of the plurality of processors (See Mason, col. 10, lines 17-33, the match-disable bit is not required to be maintained on each entry in the translation buffer. Whether or not address-space matches should be disabled is properly a function of the

execution environment of the CPU rather than of the virtual address. When the virtual machine monitor is being executed (as discussed below), address-space matches are disabled; when a virtual machine or some process in a VM is being executed, address-space matches are enabled. In another embodiment of the invention, the match-disable bit could be stored globally in the translation buffer. In yet another embodiment of the invention, the match-disable bit could be maintained in the CPU itself. In either case, its value would be changed on transition from the VMM to a VM or from a VM to the VMM, and its current value must be made available to the match comparison logic in the translation buffer).

Per claims 7-8, the 32-bit values are zero-extended into 64-bit values (col. 6, lines 31-35,

A feature of the CPU 10 of FIGS. 1-6 of this example embodiment is its RISC characteristic. The instructions executed by this CPU 10 are always of the same size, in this case32-bits, and col. 8, lines 5-9, while if bit-12 is a one then an 8-bit zero-extended literal constant is formed by bits <20:13> of the instruction. This literal is interpreted as a positive integer in the range 0-255, and is zero-extended to 64-bits).

Regarding claims 10-12, 16-18, and 22-24, it is well known in the art that a computer system can perform any kind of function (requested action) regardless of the type of action, and it does not change the way instructions and register bits are being manipulated, because the computer does not know what type of request action it is performing, therefore, these limitations does not constitute patentable limitations.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Majid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington. VA, Six Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses to the Examiner.

All Formal or Official Faxes must be signed and sent to either (703) 308-9051 or (703) 308-9052. Official faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the office, e.g., Finance Division for fee charging, etc.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Majid Banankhah

1/25/04

MAJID A. BANANKHAH
PRIMARY EXAMINER